NEPP Electronic Technology Workshop
June 22-24, 2010

National Aeronautics and Space Administration

On-Going Radiation Effects on FPGAs - Lessons Learned and Plans

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Intro: FPGAs and Single Event Effect (SEE) Susceptibility

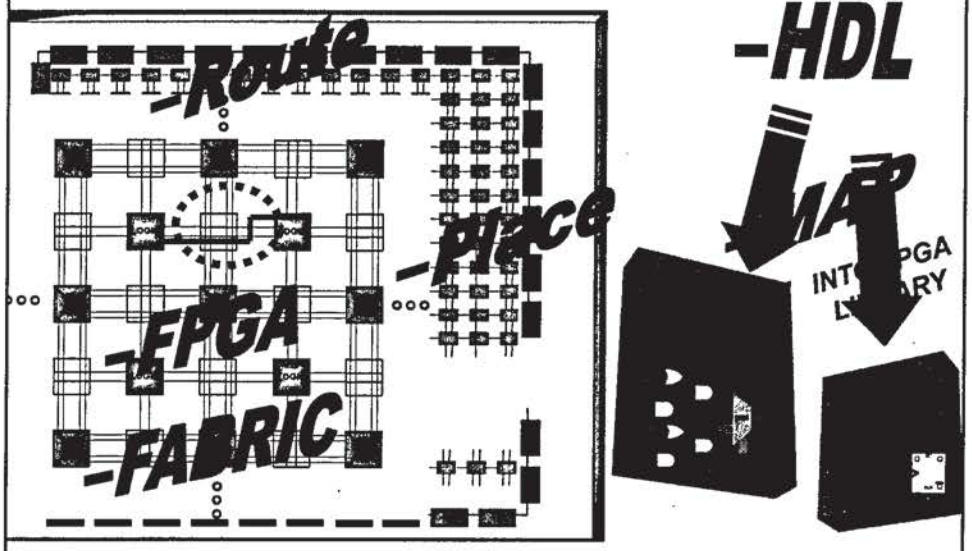
- 2 Basic elements of a FPGA device:
  - Configuration
  - Functional logic
- Both are different technology nodes with different SEE upset rates
- Building Blocks can be configured to implement complex functionality in the order of System on a chip (SOC)

Variation of building blocks and complexity of utilization (SOC) make it no longer valid to simply count upsets during SEE testing

To be presented at the 1st NASA Electronic Parts and Packaging (NEPP) Program Electronic Technology Workshop June 22-24, 2010, NASA GSFC, Greenbelt, MD.

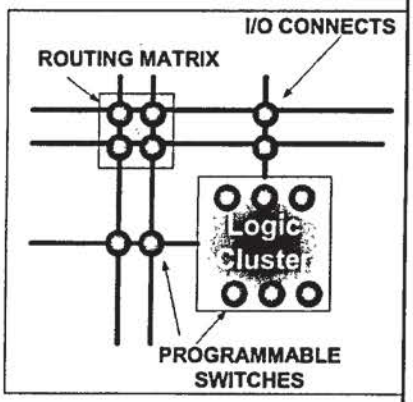
To be presented by Melanie Berg at the NASA Electronic Parts and Packaging (NEPP) Program Electronic Technology Workshop, NASA-GFSC, Greenbelt, MD, June 22-24, 2010 and published on http://nepp.nasa.gov.

FPGA Building Blocks: How Gates and Routes Are Utilized in FPGA Fabrics



Place, Route, and Gate Utilization are Stored in the FPGA Configuration

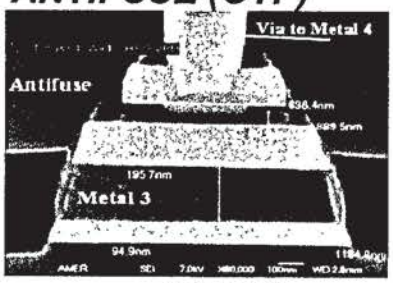
- ***Configuration Defines:***
  - ***Functionality (logic cluster)***
  - ***Connectivity (routes)***
  - ***Placement***



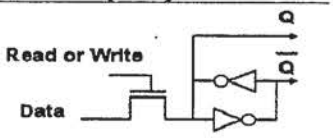
- ***Programming Switch Types:***
  - ***Antifuse: One time Programmable (OTP)***
  - ***SRAM: Reprogrammable (RP)***
  - ***Flash: Reprogrammable (RP)***

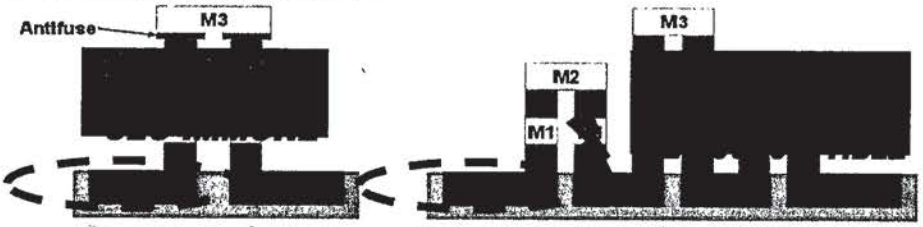
Programmable Switch Implementation and Single Event Upset (SEU) Susceptibility

ANTIFUSE (OTP)



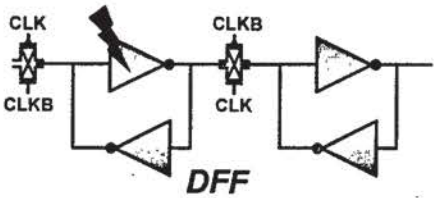
SRAM (RP)





Logic Building Block SEU and Single Event Transient (SET) Susceptibility

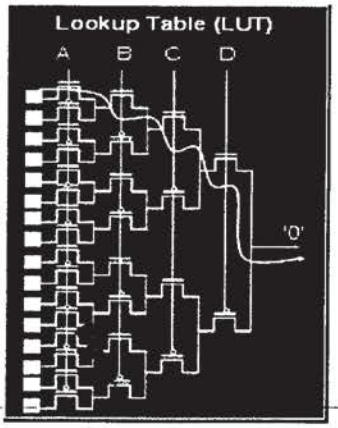
- **Logic Blocks**
  - **Flip-Flops (DFFs)**
  - **Combinatorial Logic**
  - **Global Routes (clocks and resets)**
  - **Custom internal circuitry**



DFF

SEU

Not Frequency dependent



Xilinx combinatorial logic

SET

Frequency dependent

Putting It All Together...FPGAs (SEE) Susceptibility

$$P(fs)_{error} \propto P_{Configuration} + P_{functional\,Logic} + P_{SEFI}$$

- $P(fs)_{error}$: **Design Specific SEE upset rate**
- $P_{Configuration}$: **Configuration SEE upset rate**
- $P_{functional\,Logic}$: **Functional logic SEE upset rate**
- P_{SEFI}: **Single Event functional Interrupt**

$$P_{DFFSEU} + P(fs)_{SET \rightarrow SEU}$$

SET must get captured and become an SEU

Must Clearly state which SEE type is being evaluated... Beware... sometimes difficult to differentiate

Building Blocks to Consider during SEE Testing

SEE Test Strategy

Different Technology

Configuration

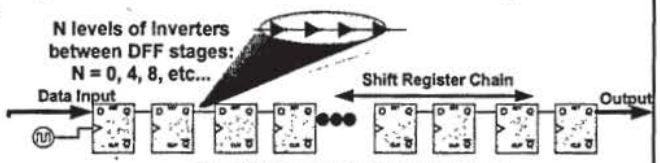
- Static
- NOT performed for Anti-fuse FPGA
- Read Back SRAM or Flash

Functional Logic

- Generally dynamic testing is required
  - DFFs and Combinatorial
  - SEFIs: Global Routes (clocks and resets)
  - SEFIs: Custom internal circuitry
- Logic blocks vary per FPGA

FPGA Design Under Test Development

- Create FPGA designs that repeat blocks to increase statistics
- Create FPGA designs that exercise and hence expose building blocks



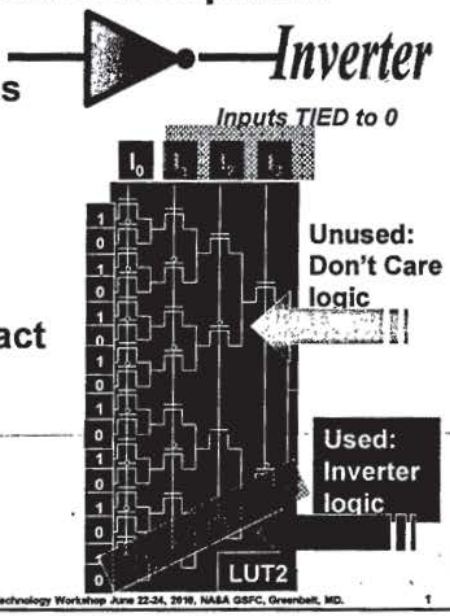
Traditional FPGA Testing

- Divide and conquer…Determine separate error cross sections that correspond to specific:
  - Frequencies
  - Designs and Building blocks (when applicable)

No one cross section or "bit-error rate" applies to an FPGA

Some Questions That Have Driven REAG FPGA Test Strategy and Development

- Are shift registers designs sufficient to expose logic level susceptibility?
  - Fanout is linear
  - Can only use inverters or buffers
- How does frequency impact SEU error cross sections



SRAM Configuration Questions:

- **For non-mitigated designs, Consortium data shows that configuration upsets are most significant**

$$P_{system} \propto P_{Configuration}$$

Xilinx Consortium: *VIRTEX-4VQ STATIC SEU CHARACTERIZATION SUMMARY: April/2008*	Probability	Error Rate	LEO	GEO
Configuration Memory: XQR4VSX55	$P_{configuration}$	$\frac{dE_{configuration}}{dt}$	7.43	4.2
Combined SEFIs per device	P_{SEFI}	$\frac{dE_{SEFI}}{dt}$	7.5×10^{-5}	2.7×10^{-5}

REAG Investigation: How does Configuration upsets scale with technology and how does mitigation (redundancy + scrubbing) impact configuration upset rates

To be presented at the 1st NASA Electronic Parts and Packaging (NEPP) Program Electronic Technology Workshop June 22-24, 2010, NASA GSFC, Greenbelt, MD.

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FY10: FPGAs
(Continuation)

Description:

The main goal of this task is to investigate FPGAs from various vendors and to determine applicability for the space radiation environment. The following is a more detailed list of task goals.

- Determine inherent radiation sensitivities of advanced complex commercial CMOS (<100 nm) and hardened FPGAs
- Provide guidance on radiation test and qualification procedures
  - As a consultant
  - Test and analysis FPGA guideline development
- Determine SEU sensitivities for hardening approaches
- Comparison of fault injection versus beam SEU coverage
- Evaluate low proton energy sensitivity of commercial CMOS FPGAs (Low Energy test methodologies are discussed in detail in another task)

FY10 Plans:

Probable Test Vehicles:
- Achronix/BAE Hardened Asynchronous FPGA RADRunner
- Achronix Commercial Asynchronous FPGA SPD60
- Spartan 6 (45nm SRAM-Based)
- Actel RTAX2000s FPGA (150nm Anti-fuse Based)
- Actel ProASIC FPGA (130nm Flash-based)

Other Work:
- Support of Crypto space evaluation of Actel RTAX-S (90nm)
- Develop guideline for interpreting FPGA SEE data

Schedule:

- Will be presented on separate slides due to number of tasks

Deliverables:

- Test reports and quarterly reports
- Expected submissions to SEE Symposium, MAPLD, and IEEE RADECS. DTRA to review prior.

NASA and Non-NASA Organizations/Procurements:

Beam procurements: TAMU, IUCF, UC Davis,
- Possible use of Berkeley Facility

Partners:

Xilinx, BAE, Achronix, NRL, Actel

Principle Investigator: GSFC-MEI/ Melanie Berg
Other participants: GSFC-MEI/Hak Kim, Mark Friendlich, Chris Perez, Anthony Phan, Tim Irwin, Christina Seidlick

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Goals

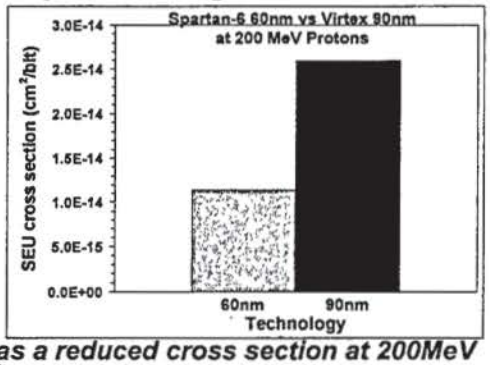
- Enhance FPGA designs under test
- Determine Functional Operation Susceptibility:
  - How often does the operation upset
  - Must perform dynamic tests
- Determine Configuration Susceptibility for:
  - Xilinx Virtex Family FPGAs
  - Xilinx Spartan Family FPGAs
  - ProASIC Flash FPGAs
- Application of upset rates:
  - Determination of dominating SEE upset rates per FPGA type
  - The role of mitigation to upset rates

Expected Impact to Community

- All test enhancements and considerations provide alternate perspectives for SEE FPGA characterization
- Results will obtain more accurate error prediction rates because device is tested and evaluated under closer to realistic circumstances

Highlights/Accomplishments: Xilinx SRAM Configuration Memory Testing

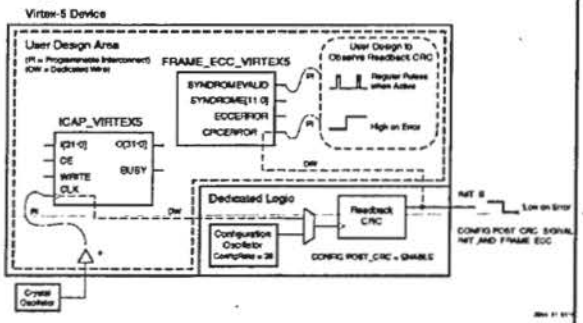
- Configuration was tested by reading back memory after irradiation:
  - Fluence had to be significant to generate enough errors for proper statistics
  - Configuration was completely static during irradiation



Technology Scaling: Spartan-6 has a reduced cross section at 200MeV Protons than the Virtex-5

Highlights/Accomplishments: Xilinx SRAM Configuration Memory and Scrubbing

- Dynamic test… Scrubber must be faster than bit error rate
- When using internal Xilinx scrubbing logic, SEFIs occur:
  - Special embedded logic used to correct configuration
  - Logic is unprotected (non-mitigated)
  - When embedded logic is upset:
    - Can write bad frames
    - Can stop working

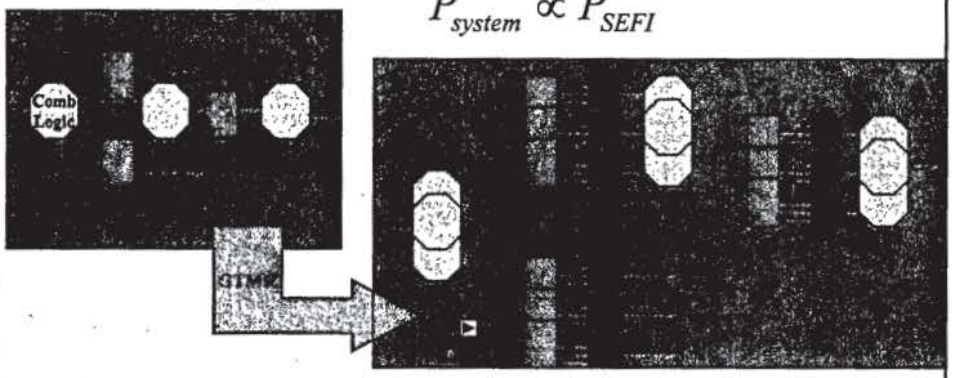


Best not to use internal non-protected Xilinx Scrub logic (e.g. Frame ECC)

Highlights/Accomplishments: Xilinx SRAM Configuration Memory and Scrubbing + Mitigation

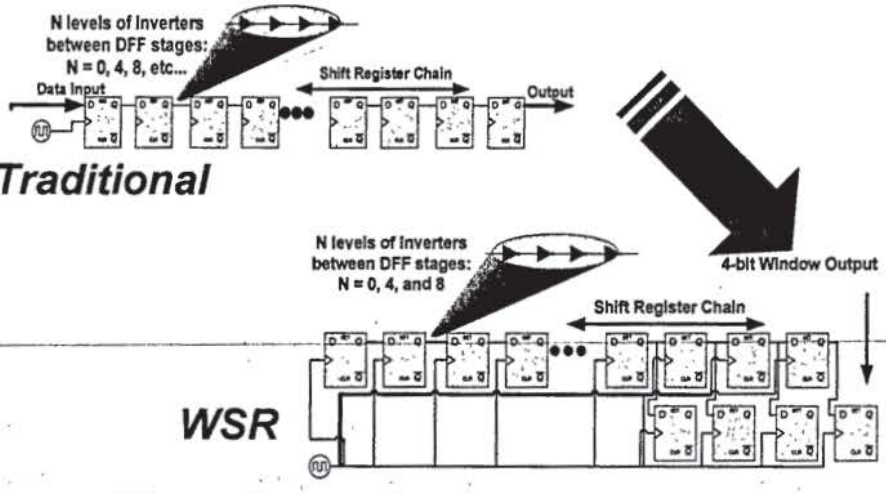
- When using Scrubbing + Global Triple Modular Redundancy (GTMR), the most significant upset rate is P_{SEFI}

$$P_{system} \propto P_{SEFI}$$

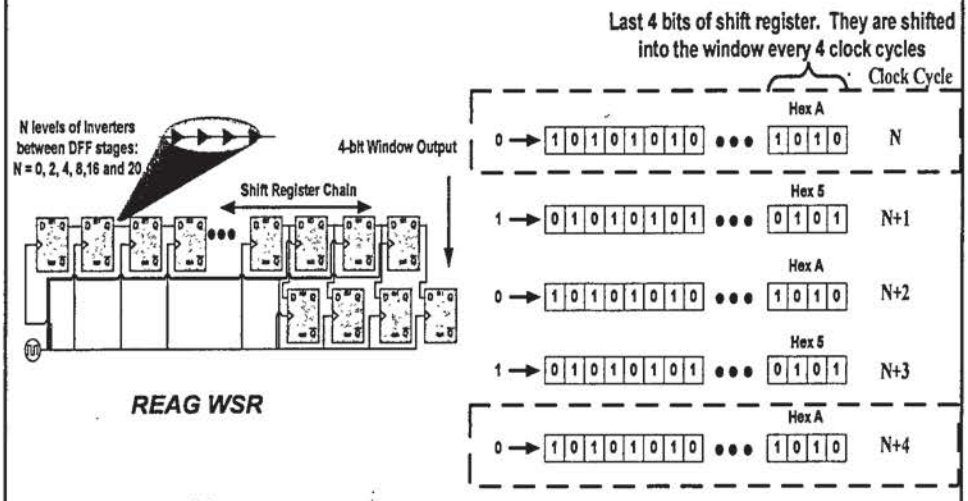


Highlights/Accomplishments: FPGA Designs Under Test

- Shift Register Enhancement: REAG Windowed Shift Register (WSR) for High Speed Signal Integrity



Highlights/Accomplishments: The WSR Advantage



Static output enhances signal integrity

Highlights/Accomplishments: REAG WSR SEE Results

- **Error rates are significantly dependent on Threshold LET(LET_{th})**
- **Choice of design impacted LET_{th}**
- **> 2 orders of magnitude in bit error rates calculations depending on data pattern and frequency of operation**

	LET_{th} >37	8< LET_{th} <30
	$dE_{bit}/dt \approx 1x10^{-10}$	$1x10^{-10} < dE_{bit}/dt < 5x10^{-8}$

Which dE_{bit}/dt do we select and How well will this bound a real design

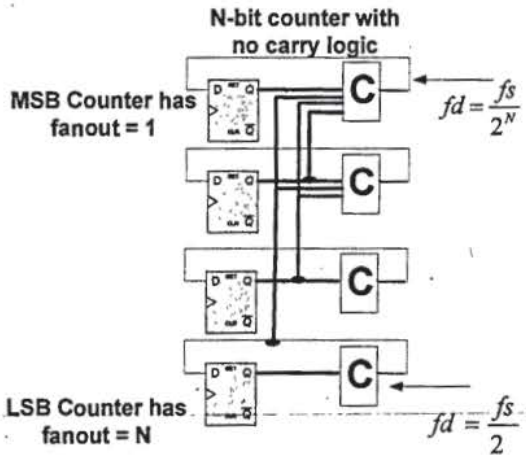
Considerations when Developing a Complex Design under Test Architecture

- It has the characteristics of a complex design with:
  - fan-out and fan-in > 1
  - contains a mixture of sequential and combinatorial logic.
- The circuit can be replicated to increase statistics.
- Its state space can be traversed within relatively short time periods such that all states are equally likely to be subject to particle strikes during radiation testing.

Counters Meet Requirements

- Has characteristics of a complex design with:
  - fan-out and fan-in > 1
  - contains a mixture of sequential and combinatorial logic.
- Variety of data pattern frequencies (f_d)
- State space Traversal = $2^N/f_s$

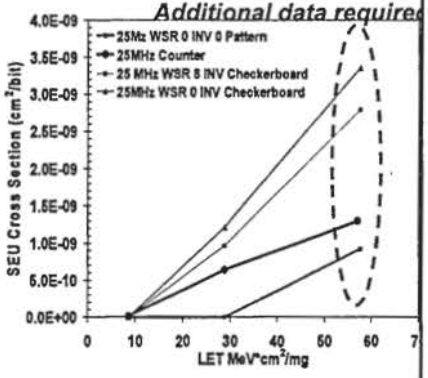
Simplified Schematic – not actual



fd: data pattern frequency
fs = system frequency

Highlights/Accomplishments:
Texas A&M Heavy Ion Results
Counters versus WSRs

- 8 inverter (INV) chains ≈ 0 INV chains at 25 MHz.
- However, as demonstrated in 2004 data, there is a significant difference in cross sections at higher frequencies.
- 23 bit counter cross section is similar to checkerboard WSR:
  - 1<= #CCells Levels<8
  - Data pattern of counter varies per bit



$$\frac{fs}{2^N} \leq fd \leq \frac{fs}{2}$$

PLANS FOR FY10/11

- Actel RTAX-s
  - Technical plans
    - May or June 2010 Heavy Ion Testing
    - Hone in on LET_{th} of the WSRs, counters, and memory modules
  - Deliverable plans
    - Update and release current Test Report (July 2010)
    - RADECs paper submission (04/01/2010)
    - SEE presentation (04/2010)
- Actel RT ProASIC (Flash Based FPGA configuration)
  - Technical plans
    - Heavy Ion and Proton Testing end of FY10
    - WSRs, counters, and memory modules (similar to RTAX-s)
  - Deliverable plans
    - Currently in discussion

PLANS FOR FY10/11 Continued

- Xilinx Spartan 6
  - Technical plans
    - Heavy Ion and low energy Proton Testing end of FY10
    - WSRs and counters with and without mitigation
  - Deliverable plans
    - Indiana University -Proton Test Report 04/2010
- Achronix RadRunner
  - Technical plans
    - Laser Testing 5/2010
    - WSRs, counters, and embedded memory
  - Deliverable plans
    - Depends on test completion

SCHEDULE

	Microelectronics	2009			2010								
	T&E	O	N	D	J	F	M	A	M	J	J	A	S
Actel RTAX-s	On-going discussions for test samples												
	Radiation Test Development and Testing												
	Data Evaluation and Test reports												
	Paper Submission												

Schedule

	Microelectronics T&E	2009 O	N	D	2010 J	F	M	A	M	J	J	A	S
BAE/ Achronix FPGA	On-going discussions for test samples												
	Radiation Test Development												
	Test Devices and reports												
	Paper Submission												

Schedule

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Achronix FPGA	On-going discussions for test samples												
	Radiation Test Development												
	Test Devices and reports												
	Paper Submission												

Schedule

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Spartan6	On-going discussions for test samples												
	Radiation Test Development												
	Test Devices and reports												
	Paper Submission												

Schedule

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Actel ProASIC	On-going discussions for test samples												
	Radiation Test Development												
	Test Devices and reports												
	Paper Submission												

What Did We Learn So Far?

- Must take into account:
  - System Frequency
  - Data Pattern
  - Levels of logic between DFFs
- Complex testing demonstrated that checkerboard WSR SEE error rates obtained at a similar frequency may provide a sufficient upper bound for complex circuits
- Counter + WSR testing revealed the non-linear relationship of frequency, LET, capacitance, and individual bits.
- Current evaluation includes formulating cross sections per bit to make a direct comparison with similar WSR chains.
- We need more data for analysis

SEE Radiation Testing Challenges

- Difficult to identify upsets
- Difficult to capture high speed upsets or bursts
- Difficult to differentiate upsets
- Difficult to create and operate designs that will expose SEEs compatible with normal operation in space
- Difficult to test comlex circuitry in an accelerated environment